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GTO thyristor and bipolar transistor cascode switches

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Abstract: The switching performance of both the bipolar transistor and gate turnoff thyristor is improved when used in a cascode switch configuration. 'Snubberless' turnoff occurs without second breakdown and the technique results in shorter saturation delay times, faster current fall and higher operational sustaining voltages than obtained with conventional switching techniques. Improved switching performance is traded for increased drive circuit complexity and an increased on-state power loss associated with two series connected power semiconductor switches. The circuit techniques features and performance of two 720 V DC, 320 A cascode switches are presented. The bipolar transistor cascode switch is tested up to 100 kHz, whereas tail current power loss limits the GTO thyristor cascode switch to 16 kHz.

1 Introduction

The switching performance of snubberless cascode connected bipolar devices has been extensively investigated. The snubberless 'emitter' switch, using a fast switching low-voltage MOSFET or bipolar transistor in series with the emitter of a high-voltage bipolar transistor has been shown at turnoff to give reduced storage and current fall times [1–7]. At turnoff, the emitter of the high voltage transistor is open circuit, thereby preventing reverse bias second breakdown. All the collector current is diverted to the base, and the switch undergoes fast and safe square load-line switching within the safe operating area bounded by the collector-to-base breakdown voltage. The consistency in turnoff characteristics, including temperature effects, was considered at high voltages, but at currents below 20 A [1]. Recent work by the authors significantly increased the emitter switch rating to 600 V DC and 100 A switching at 20 kHz [7]. A 'snubberless' 720 V DC, 320 A, 100 kHz, bipolar transistor emitter switch is presented in this paper. Available bipolar transistors will allow these ratings to be extended to figures in excess of 1000 V DC and 500 A at 100 kHz. The 1000 V DC limit can only be practically exceeded by using GTO thyristor technology.

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The 'rec cathode' switch, using a GTO thyristor (GTO) in series with a low-voltage diode in the cathode and incorporating a conventional *RCD* turnoff snubber, has been operated at 610 V DC and 550 A giving improved GTO turn off characteristics [8], albeit at a low switching frequency. A snubberless 'cathode' switch, using a high-voltage GTO thyristor in series with a MOSFET in the cathode, was initially demonstrated at low voltage and current levels of 270 V DC, 10 A [9]. These limits were extended to 500 V DC and 300 A for a single pulse [10]. A 'snubberless', 720 V DC 320 A, 16 kHZ, GTO cathode switch is presented here and in References 11 to 13.

The turnoff requirements for the emitter switch and the cathode switch are very similar, whereas the turnon base requirements for the emitter switch are complicated by low transistor gain. Switch robustness is achieved by the elimination of current pinching at turnoff because the cathode or emitter is open circuit, and thus second breakdown is prevented. GTO tail current associated power loss and dissipation constraints, limit the cathode switch upper operating frequency.

2 Basic cascode switch configurations

Fig. 1 shows two simplified cascode switch configurations, one using a bipolar transistor as the high-voltage switching element, Fig. 1*a*; the second circuit, Fig. 1*b*, using the GTO thyristor as the main switching element. The turnoff circuits are the same for both switch types. In each case turn off of the main switching element, T_1 is achieved by simultaneous

(*a*) removal of the steady-state on-drive current I_{on}
(*b*) turnoff of the cascode MOSFET T_c
(*c*) turnon of the clamp MOSFET T_s

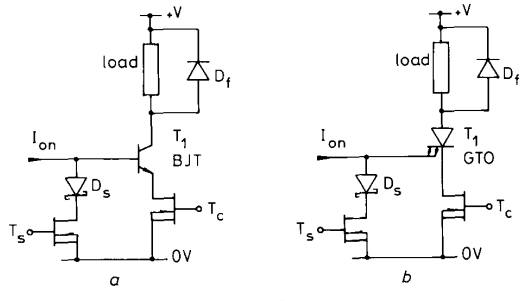

Fig. 1 *Basic cascode switch configurations*
a Emitter switch using bipolar junction transistor
b Cathode switch using gate turnoff thyristor

At turnoff the load current is diverted from T_c to the clamp MOSFET T_s and the high-voltage bipolar switch T_1 turns off with unity reverse current gain. The bipolar transistor acts like a diode as the collector junction recovers, whereas the GTO behaves like a *pnp* transistor turning off in the V_{ceo} mode, or a V_{cer} turnoff mode if anode shorts are incoporated. The Schottky diode D_s prevents reverse current through the cascode switch when used in a bridge-leg configuration.

At turnon, the load current is diverted from the load freewheel diode D_f to the cascode switch by simultaneous

(*a*) application of the on-drive current I_{on}
(*b*) turnon of the cascode MOSFET T_c
(*c*) turnoff of the clamp MOSFET, T_s

3 Voltage clamps and snubber circuits for the cascode switch

Similar anode and collector associated circuits are used on both the GTO thyristor and bipolar transistor cascode switches. A combination of turnon snubbers, *RC* turnoff snubbers and turnoff voltage clamps are used as shown in the circuit of Fig. 2. These circuits reduce switching stress and absorb energy associated with stray inductance. The conventional *RCD* turnoff snubber is not used.

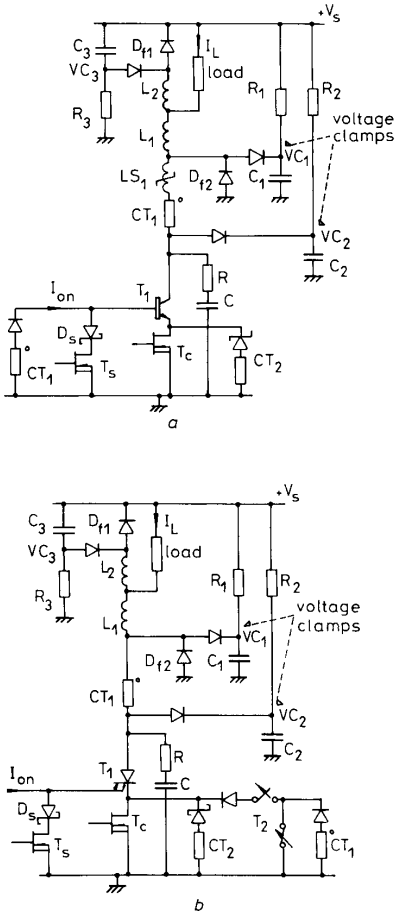

Fig. 2 *Cascode switch circuit diagrams*
a Emitter switch
b Cathode switch

3.1 Linear inductor turn on snubber

The air-core inductor $L_1 + L_2$ controls the reverse recovery di/dt of diode D_{f1} at switch turnon, according to $di/dt = V_s/L$. A byproduct of this function is a reduction in switch loss at turnon. The turnon inductor is shown in Fig. 2 in two parts, L_1 and L_2, so as to provide the correct functions for a bridge-leg configuration.

3.2 Voltage clamps

At turnoff, the load current transfers to the freewheel diode D_{f1} and $\frac{1}{2}(L_1 + L_2)I_L^2$ is dissipated in the voltage clamp resistor R_1. Because of the energy stored in $L_1 + L_2$, the capacitor C_1 voltage increases and the reset current flows through R_1 into the supply V_s. The parasitic inductance of R_1 has a significant effect on the amplitude of the capacitor reset current. The maximum switching frequency is limited to about $1/3R_1C_1$ Hz. Typical inductor current and capacitor voltage waveforms are shown in Fig. 3.

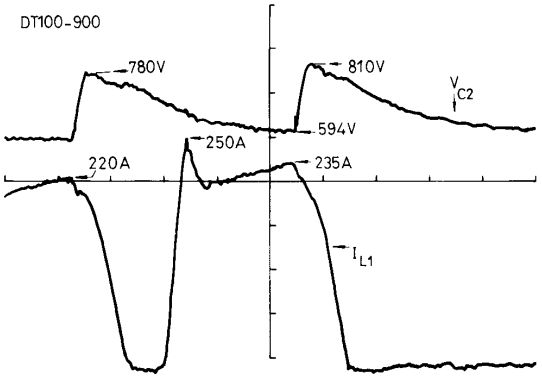

Fig. 3 *Voltage clamp waveforms*
Upper trace: Capacitor C_2 voltage, 150 V/div
Lower trace: Inductor L_1 current, 50 A/div
} time scale = 3μs/div
V_{RAIL} = 600 V

A second function of the voltage clamp is to control voltage overshoot during freewheel diode reverse recovery. A procedure exists to produce an optimal design voltage clamp [14].

3.3 Saturable reactor turnon snubber

The saturable reactor LS_1 used only on the emitter switch, performs a turn on snubber function, supporting voltage during the collector voltage fall until the core saturates. After the collector reaches a low voltage, the core saturates and the collector current rises rapidly. This component can be dispensed with if turnon loss is acceptably low.

3.4 Current transformer

The current transformer CT_1 in Fig. 2 provides the main proportional base drive for the bipolar transistor and negative cathode current for the GTO at turnoff. It is not essential for the cathode switch, but convenient.

At switch turn off LS_1 and CT_1 are reset by the voltage clamp VC_2. As with L_1, stored energy is transferred to the voltage clamp and dissipated in R_2. It is arranged by the value of capacitance, and the relative levels of stored energy in each magnetic component, that the voltage of clamp VC_2 is greater than that of clamp VC_1 for a specified time. This allows CT_1 and LS_1 to reset [11]. The voltage reached by VC_2 must be less than the breakdown voltage of the main switch T_1.

The total inductance in series with the collector is 3 μH of which 2.2 μH is contributed by $L_1 + L_2$ and the remaining 0.8 μH is due to the current transformer CT_1, saturable reactor LS_1 and stray inductance. The value of the centre tapped inductor $L_1 + L_2$ is decreased to 1 μH for the cathode switch.

The reset of CT_1 and LS_1 is protracted by an apparent increase in inductance as the current in each element reaches its magnetising current level. The time constant of the LC oscillation between the inductance of CT_1 plus LS_1 and C_2 is subsequently extended. Consider the current transformer model in Fig. 4.

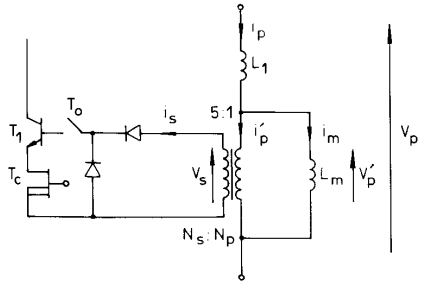

Fig. 4 *Model for current transformer CT_1*

The magnetising current i_m increases linearly and is related to the secondary voltage v_s according to

$$v'_p = v_s/5 = L_m \frac{di_m}{dt} \tag{1}$$

To prevent saturation it is essential to reduce i_m to zero during the switch off time. The primary current i_p is increased above that required for secondary current i_s by the magnetising current i_m, i.e.

$$i_p = i_m + 5i_s \quad (= i_m + i'_p) \tag{2}$$

In resetting the CT the first stage is to reduce the secondary current i_s hence i'_p to zero. The primary current i_p is reduced to the magnetising current level i_m. When the secondary current reaches zero, the LC oscillation circuit changes from C_2 and L_l to C_2 and $L_l + L_m$. The quarter period of oscillation is effectively increased from $\frac{1}{2}\pi\sqrt{(L_l C_2)}$ to $\frac{1}{2}\pi\sqrt{[(L_l + L_m)C_2]}$.

Eqn. 2 shows that at low primary current levels the magnetising current must be minimised, which is achieved by maximising the magnetising inductance L_m. But to minimise the current reset quarter-period oscillation, the magnetising inductance must be minimised.

The total off time, before switch turnon can safely be initiated, is 2.6 μs, and comprises 0.6 μs for the maximum storage time and voltage rise time and 2 μs for resetting the CT and saturable reactor.

3.5 RC snubbers

Inductance unclamped by the voltage clamps VC_1 and VC_2, resets in a small, low inductance RC snubber (1 Ω, 10 nF) across the cascode devices T_1 and T_c.

On a 700 V DC rail, switching the GTO at 16 kHz, from CV^2f, a 78 W, 1 Ω snubber resistor is notionally required. Such a bulky resistor would have significant parasitic inductance, rendering the RC circuit ineffective. Fortunately the 78 W power dissipation requirement is not applicable, and less than 20 W is acceptable up to 50 kHz.

The GTO cathode switch anode voltage rise and fall times t_f are typically 200 ns. Since the RC circuit has a very short time constant (τ = 10 ns) minimal loss occurs in the snubber resistor during anode voltages rise and fall periods [15]. Resistor loss is approximated by

$$P_R \simeq \frac{\tau}{\tau + t_f} CV^2f = 3.8 \text{ W} \tag{3}$$

The primary function of the RC snubber is to absorb the energy associated with stray inductance L_s. The RCL circuit formed is critically damped to minimise the voltage overshoot as the energy stored in inductor L_s is dissipated in the resistor. This damping function becomes active when the anode voltage exceeds the DC supply rail voltage at turnoff. Resistor power loss at 300 A, with 7 nH of unclamped stray inductance is given by

$$P_R = \tfrac{1}{2}L_s I^2 f = 5 \text{ W} \tag{4}$$

The total resistor power loss is therefore 5 + 3.8 = 8.8 W.

At switch turnon, almost all the energy stored in the RC-snubber 10 nF capacitor, 36.2 W of 40 W, is dissipated in the GTO. If a linear voltage fall is assumed, from $i = C\,dV/dt$, a 35 A square wave current flows for the 200 ns voltage fall time. Since inductive turnon snubbers are used, switch turnon loss due to the load current is minimal.

At switchoff the 10 nF capacitor acts to divert current from the switching device. The bipolar switch loss during current fall is decreased, depending on the current fall time. At rated current 320 A, on a 720 V DC rail, bipolar switch turnoff loss is decreased. The extra 36.2 W of turnon loss is therefore compensated for by the decrease in turnoff loss.

The snubber is distributed in two RC circuits, each consisting of 4.7 nF + 2 Ω, where the 2 Ω resistance is made up of five 10 Ω, 2 W carbon composition, high working voltage, low inductance resistors. For high dv/dt capability, 4.7 nF, 2000 V metallised polypropylene capacitors were used.

4 Bipolar transistor emitter switch

Fig. 5 shows a detailed circuit diagram for the bipolar transistor emitter switch that has been examined at 720 V DC, 320 A at switching frequencies in excess of 50 kHz. The *npn* bipolar junction transistor used to obtain these ratings was a DT500–1000, which is a 400 A, 900 V, 44 mm diameter triple diffused discrete device.

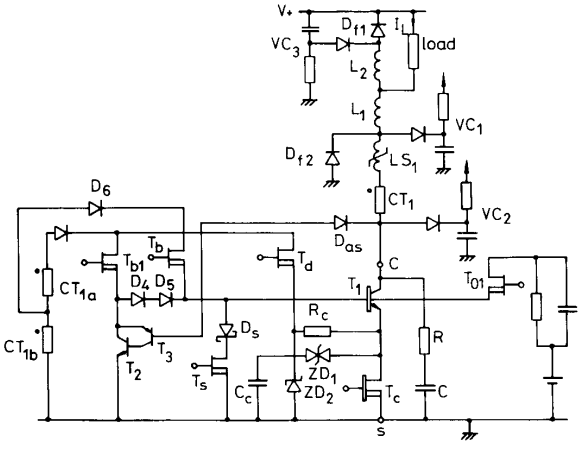

Fig. 5 *Detailed circuit diagram of emitter switch*

The ideal collector voltage and current switching cycle waveforms shown in Fig. 6 are used to illustrate various circuit features and operational details.

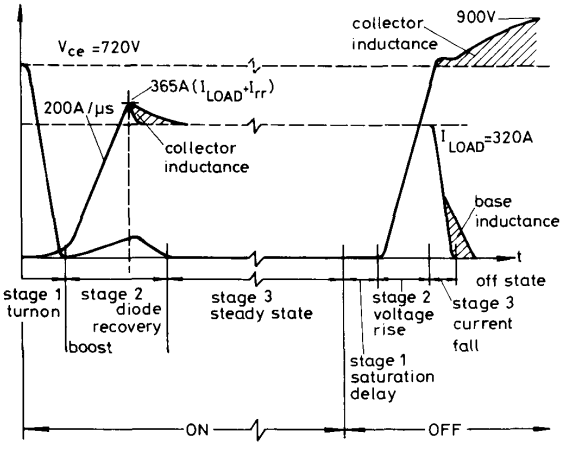

Fig. 6 *Collector voltage and current waveforms showing turnon and turnoff stages*

4.1 Turnon

A three stage, optimal, adaptive base drive circuit is used to bring the transistor into conduction and to avoid overdrive, which would result in prolonged saturation delay at turnoff, particularly with very short on times.

Before turnon, the inductive load current I_L flows through the freewheel diode D_{f1}. The transistor emitter switch is brought into conduction by simultaneous

(*a*) turnoff of the clamp MOSFETs T_s

(*b*) turnon of the emitter MOSFETs T_c and the base-drive MOSFET T_{01}

4.1.1 Stage 1, voltage fall: A 20 A current pulse established at 400 A/μs is fed into the transistor base via T_{01}. After a turnon delay t of 100 ns, the collector voltage falls to below 8 V in less than 200 ns (t_{fv}) at which time the 20 A turnon pulse is removed within 30 ns. The saturable reactor LS_1 restricts the collector current to the reactor magnetising current for 200 ns while the collector voltage falls to near zero.

Detection of the low collector voltage on-state condition (<8 V) is performed by the very fast detection circuit shown in Fig. 7*a*. The temperature independent, high voltage threshold of 74AC technology is used as a fast, low current, inexpensive collector voltage level detector. The output signal of the circuit in Fig. 7*a* is used to turnoff the MOSFET T_{01}.

The adaptive removal of the 20 A start pulse as the collector voltage falls to <8 V, ensures the base of any transistor has been provided with optimal base charge. All the delivered base charge is used in reducing the collector voltage as junction capacitances are charged. Prolonged saturation delay at turnoff is avoided at very low collector currents.

4.1.2 Stage 2, freewheel diode reverse recovery: The air core multistrand wound inductor $L_1 + L_2$ controls the initial collector di/dt to 200 A/μs as the freewheel diode D_f recovers as shown in Fig. 6. The boost winding CT_{1b} of the current transformer CT_1 is connected to the base via MOSFET T_b. A base current of 40% of the collector current magnitude attempts to compensate for the diode high recovery current. The high di/dt collector current causes the transistor to desaturate, reaching a maximum collector voltage at the peak of the diode recovery current.

Given the very wide collector current range, 0 to 320 A, it is not possible to actively control the base current during diode recovery so as to prevent the transistor from leaving the saturated on state. The instantaneous base current $i_b(t_o)$ is proportional to the collector current $i_c(t_o)$, neglecting any current transformer magnetising current, that is

$$i_b(t_o) = 0.4 i_c(t_o) \tag{5}$$

The base current causes electrons to be injected from the n^+ emitter into the p-base region. Electrons take a finite time τ_B to traverse the effective base width W_B and reach the collector space charge layer, SCL. The base transit time τ_B is given by [16]

$$\tau_B = W_B^2/2D_n \tag{6}$$

where the diffusion constant $D_n(10^{16}/\text{cc}) = 35\ \text{cm}^2/\text{s}$ and the effective base width $W_B = 18\ \mu\text{m}$. The transit time from emitter SCL to collector SCL is therefore 50 ns.

Electrons associated with the base current $i_b(t_o)$ reach the collector at time $t_o + \tau_B$, by which time the collector current has increased from $i_c(t_o)$ to $i_c(t_o + \tau_B)$,

$$i_c(t_o + \tau_B) = i_c(t_o) + \tau_B \cdot di/dt \tag{7}$$

which at 200 A/μs recovery current means the collector current has increased by 10 A and insufficient electrons are at the collector. The collector voltage rises, with the collector junction SCL penetrating into the base until a sufficiently high minority carrier charge is reached. Effectively the base width W_B decreases between the emitter junction SCL and collector junction SCL, hence the base transit time decreases according to eqn. 6. Since the current gain α is inversely proportional to W_B^2, as the collector voltage increases, the transistor gain increases, thereby compensating for the increase in collector current.

The traditional approach to control of the base current and hence the collector voltage is to use a Baker clamp. At these high power levels, the developed Baker clamp used to control the transistor in a steady state proved too slow, despite having a submicrosecond response as a result of low circuit inductance.

Using a proportional base drive during high collector-current di/dt cannot practically provide optimal base current conditions. Using a higher proportion of the collector current would unnecessarily prolong saturation delay when operating in the transistor's high gain mid-current region. The current transformer ratio is selected so that at maximum collector current, the forward bias safe operating area (FBSOA) V_{ce} limit is not exceeded. The FBSOA is bounded up to 50 V by a maximum collector current of 500 A. The associated on-state loss increase must be acceptable. At a collector current of 365 A, which includes a diode recovery current of 45 A, a collector voltage rise to 40 V was deemed acceptable.

After the freewheel diode peak recovery current, the collector voltage falls, as shown in Fig. 6. Excess energy is stored in the inductances L_1, L_2, LS_1 and the leakage inductance of CT_1 due to diode recovery. The excess energy in L_1 and L_2 charges the voltage clamp, VC_3, as the current in L_1 falls from $I_L + I_{rr}$ to I_L and the current in L_2 falls from I_{rr} to zero. The current in LS_1 and CT_1 decays from $I_L + I_{rr}$ to I_L in the path LS_1–CT_1–T_1–T_c–D_{f2}. The inductance of LS_1 and CT_1

should be minimised to reduce semiconductor power loss in the low-voltage discharge loop, and to minimise the current decay time. A portion of the energy stored in CT_1 and LS_1 is transferred to the load when the load voltage is increased as the voltage clamp VC_3 charges.

The current-transformer circuit in Fig. 7*b* is used to detect the freewheel diode peak recovery current instant. The circuit is electrically isolated and detects a change in sign of di/dt. Since the secondary voltage is very low and core saturation can occur after 1.8 μs, a very small ferrite transformer core can be used. Following a fixed delay, the circuit is used to reactivate the linear detection circuit in Fig. 7*a*, and after diode recovery, when the collector voltage has fallen to 8 V, switch T_b is turned off and T_{b1} is turned on. That is, the 40% I_c boost base current is turned off and 20% I_c base current is used.

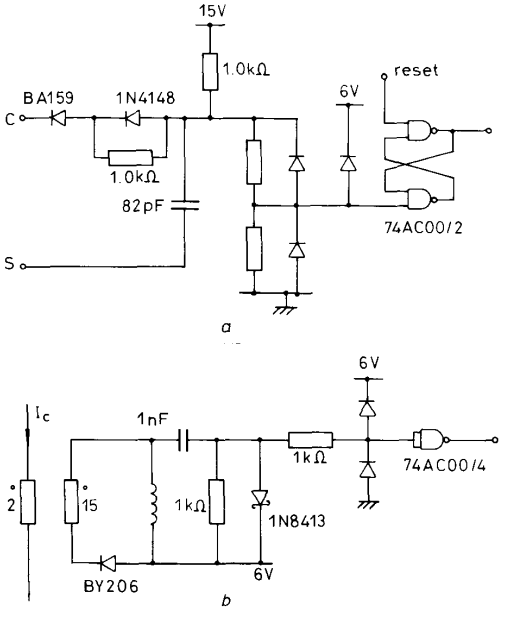

Fig. 7 *Collector detection circuits*
a Linear detection circuit
b Diode recovery detection circuit

4.1.3 Stage 3, steady state: The base current is controlled by the novel high-speed shunt regulator shown in Fig. 8, which maintains the emitter switch collector voltage at any desired level.

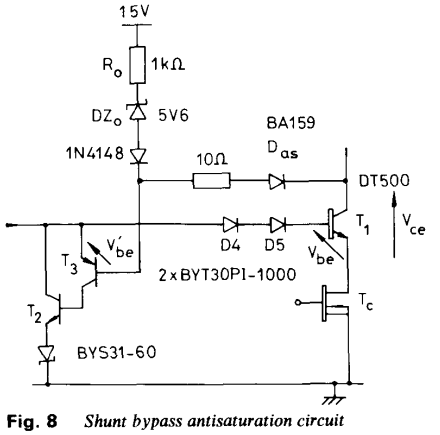

Fig. 8 *Shunt bypass antisaturation circuit*

The collector voltage is sensed via a low current high-speed high-voltage diode D_{as} which controls the shunt complementary transistor pair T_2 and T_3. The base diodes D_4 and D_5 set the collector on state voltage level to 3 V, according to

$$V_{D4} + V_{D5} + v_{be} = v'_{be} + V_{Das} + v_{ce} \quad (8)$$

The shunt circuit is prebiased to an off state by R_o and DZ_o to give good stability and a high bandwidth.

An antisaturation circuit renders the turnoff period less sensitive to variation in collector current, conduction period, temperature and transistor production tolerances. The conventional antisaturation circuit, the Baker clamp, can shunt significant base current into the collector because of the wide variation in gain with collector current and temperature. In nonDarlington configurations, the collector diode D_{as} of the Baker clamp is a high-current high-voltage high-speed device. At transistor turnoff, the reverse recovery current from the diode D_{as} is injected as noise into the base circuit. In Fig. 8 the diode D_{as} which completes a feedback connection, only conducts a low current. Hence, little recovery current results. No injected noise problems are incurred. A low sensing current results because of the very high gain (2500) of the low-voltage shunting transistors T_2 and T_3.

4.2 Base-drive modifications

To provide optimal base current for the bipolar transistor, a three stage adaptive drive circuit is used. The minimum switch on time is set to 0.5 μs at full current rating to limit any instability. The switched maximum on time is set by the saturation time of the current transformer CT_1, designed to be greater than 62 μs, which is suitable for 16 kHz and ultrasonic switching.

Base-drive circuit complexity can be significantly simplified with little degradation in performance for many applications, particularly if the switching frequency is less than 20 kHz.

The current transformer CT_1, 40% boost winding and associated circuitry may be omitted, by increasing the magnitude and duration of the start pulse to cover the maximum expected time to the peak of freewheel diode reverse recovery. The 20% I_c base current is provided simultaneously with the uncontrolled start pulse.

The shunt regulator and associated antisaturation circuitry may be dispensed with since turnoff occurs with unity reverse gain. Saturation delay will increase, particularly at low collector currents, and turnoff loss is increased due to the increase in voltage rise time.

If losses are not a limitation, the collector circuit saturable reactor LS_1 is dispensable.

By simplifying the base drive circuitry a significant reduction to the control logic circuitry results.

4.3 Turnoff

The load current I_L is diverted from the emitter switch to the freewheel diode D_{f1} by simultaneous

(*a*) turnoff of the MOSFETs T_c and T_{b1} (T_b is already off)

(*b*) turnon of the clamp MOSFETs T_s and the base current diverting MOSFET T_d.

The collector linear detection circuit, Fig. 7*a*, is disabled. A number of turnoff stages occur as shown in Fig. 6.

4.3.1 Stage 1, saturation delay: The transistor emitter current is diverted to the base and through the shunt T_s at over 1000 A/μs. To attain this high current diversion

rate, the stray inductance in the loop formed by T_c, the base and emitter of T_1, D_s and T_s must be low. A high reverse base current transfer rate significantly reduces the saturation delay time. The special biasing network across the drain to source of the emitter MOSFET T_c lifts the emitter potential to 45 V. With 40 nH stray inductance, the emitter current is forced into the base at over 1125 A/μs.

During the turnoff process there must be no forward base current if failure of bipolar transistor T_1 is to be prevented. Practically, reverse emitter current should flow to swamp any parasitic base current oscillations during the transfer of the emitter current.

To meet this requirement three circuit aids have proved desirable:

(i) While the collector current continues to flow, the current transformer action of CT_1 must be preserved. At turnoff the base current from the current transformer is diverted into the emitter-drain connection of the emitter switch via MOSFET T_d and Zener diode ZD_1. The diverted current gives a reverse emitter current, flowing through the clamp MOSFET T_s until the emitter junction recovers. The charge required for the emitter junction to recover is dependent on the forward current previously flowing and, likewise, so is the reverse emitter current, by current transformer action. Thus the reverse drive is adaptive and forces the emitter junction to recover before transistor T_1 turns off. The emitter junction cannot support a voltage until it has recovered and consequently the emitter is held at zero potential by the clamp MOSFET T_s. The emitter voltage falls from 45 V to zero potential as the emitter current falls through zero to the negative current transformer level. As the emitter junction recovers it will support a voltage up to its avalanche breakdown of typically 18 V. At this point the current from CT_1 is diverted to the lower voltage clamp path, ZD_2.

(ii) At low collector current levels and at the end of turnoff a small current transformer CT_2 maintains a reverse emitter current in case the emitter junction has not fully recovered. During turnoff, very high di/dt values, in association with stray inductance, lead to large voltage transients. Therefore a current transformer was used to maintain a steady reverse current pulse of 5 A for 1.5 μs during any voltage transitions.

(iii) During the off period the RC snubber formed by R_c and C_c, and the MOSFET T_c output capacitance, provides a steady state reverse leakage current to maintain a reverse biased emitter junction.

4.3.2 Stage 2, collector voltage rise: When the saturation charge in the collector n-region has been removed, the collector voltage rises as shown in Fig. 6. Since the emitter has already cut off, the collector voltage rises, ultimately, at over 5000 V/μs without second breakdown. The collector current is yet to fall.

The voltage rise time is significantly increased if turnoff is initiated from a deep saturation state. Because of the very large excess minority base charge, the SCL penetration is slowed for a given collector current. The final portion of the voltage rise is linear and is dominated by the charging of the transistor collector junction depletion capacitance.

4.3.3 Stage 3, current fall: Once the collector voltage exceeds the rail voltage, the collector current, and hence the reverse base current, falls at over 3000 A/μs. Inductance produces package base-terminal voltage transients of up to 40 V and down to -60 V for short intervals. The collector junction of the transistor T_1 behaves like a diode with a hard recovery characteristic. Once sufficient charge has been removed through the base circuit, the collector junction rapidly recovers and snaps off. Current flowing in the 40 nH of stray inductance L_b of the base clamp circuit continues to flow, adopting a release path through the parasitic diode of the cascode MOSFET T_c and the emitter junction of T_1, which avalanches. The stored energy $\frac{1}{2}L_b I_L^2$ is dissipated in the emitter junction as shown in Fig. 6. Stray inductance must be low to prevent excessive emitter junction loss. Release of this stored energy ensures the emitter is reverse biased.

5 Emitter switch performance

Typical switching waveforms are shown in Fig. 9. Fig. 9*a* shows the three stages of the base turnon current and the resultant collector waveforms are shown in Fig. 9*b*. Turnon loss is minimal due to the action of the saturable reactor LS_1, which delays the current rise until the collector voltage has fallen. Collector desaturation to 30 V is produced at diode recovery.

Turnoff waveforms are shown in Fig. 9*c*. Current measurement in the collector was not possible because of the inductance effects introduced by the current probe. An indirect measurement approach is used involving monitoring the base current, at the base terminal. Fig. 9*c* shows that the collector current transfers to the base at just over 1000 A/μs. A high transfer rate is essential in order to minimise the saturation delay time.

Also of importance for minimal saturation delay time and voltage rise time is the on-state collector to emitter voltage, as shown in Figs. 9*d* and *e*. The collector voltage rise time t_{rv} increases with decreased $v_{ce(sat)}$. It is important to use crossover time rather than the more commonly specified current fall time in assessing switch performance. An antisaturation circuit reduces the time of the initial parabolic voltage rise. The risetime to 50% of the rail voltage takes between 70 to 80% of the total rise time. The final part of the high dv/dt voltage rise is linear as the collector current charges the collector junction depletion capacitance.

All turn off characteristics are dependent on the on-state collector to emitter voltage, which is adjusted by the number of series base diodes, D_4 and D_5, in Fig. 8. Fig. 10 shows the turnoff characteristics for different saturation levels before turnoff. The number of biasing diodes is given by the parameter K. These graphs show that an antisaturation circuit decreases storage time, Fig. 10*a*, crossover time, Fig. 10*b* and voltage rise time, Fig. 10*c*, while the current fall time, Fig. 10*d* only slightly increases with the $v_{ce(sat)}$ level. Although a high $v_{ce(sat)}$ increases on-state loss, the high frequency switching loss is decreased due to decreased voltage rise time, Fig. 10*e*.

Three transistors of similar voltage rating, but different current ratings are characterised at turnoff, with $K = 2$, in Fig. 11. The three devices are characterised in Table 1 of Appendix 15.

At turnoff a short duration voltage overshoot occurs due to unchanged collector inductance, as shown in Fig. 9*c*. This high voltage is coincident with the fall in collector current. This voltage was constrained to be greater than the V_{cer} rating, but for safety less than the V_{cex} limit, at maximum current. The smaller area lower current devices produce a larger overshoot. Variation of

the supply voltage, between 500 V and 700 V, did not result in any significant change in turnoff parameter values. The voltage rise time increases slightly with increased supply voltage.

The DT47-1050 was tested to 140 A. The saturation delay was decreased to less than 800 ns from the rated 3.5 μs, while the current fall was decreased to under 40 ns from the rated 1 μs.

The DT100–900 was extensively tested. The saturation delay was deceased from the rated 8 μs to under 750 ns and the current fall time was reduced from the rated 1 μs to less than 100 ns at higher currents, up to 260 A.

The DT500–1000 was tested to 720 V DC and 320 A. This being the equipment limit. The storage time was maintained below 700 ns and very short voltage rise times are produced as shown in Fig. 11*b*.

6 GTO thyristor cathode switch

At turnoff the GTO suffers from a long storage time and current fall time as well as a prolonged current tail. Nonetheless, it has advantages over the bipolar transistor. The gate on drive requirements are relatively simple and power handling capability in a similar

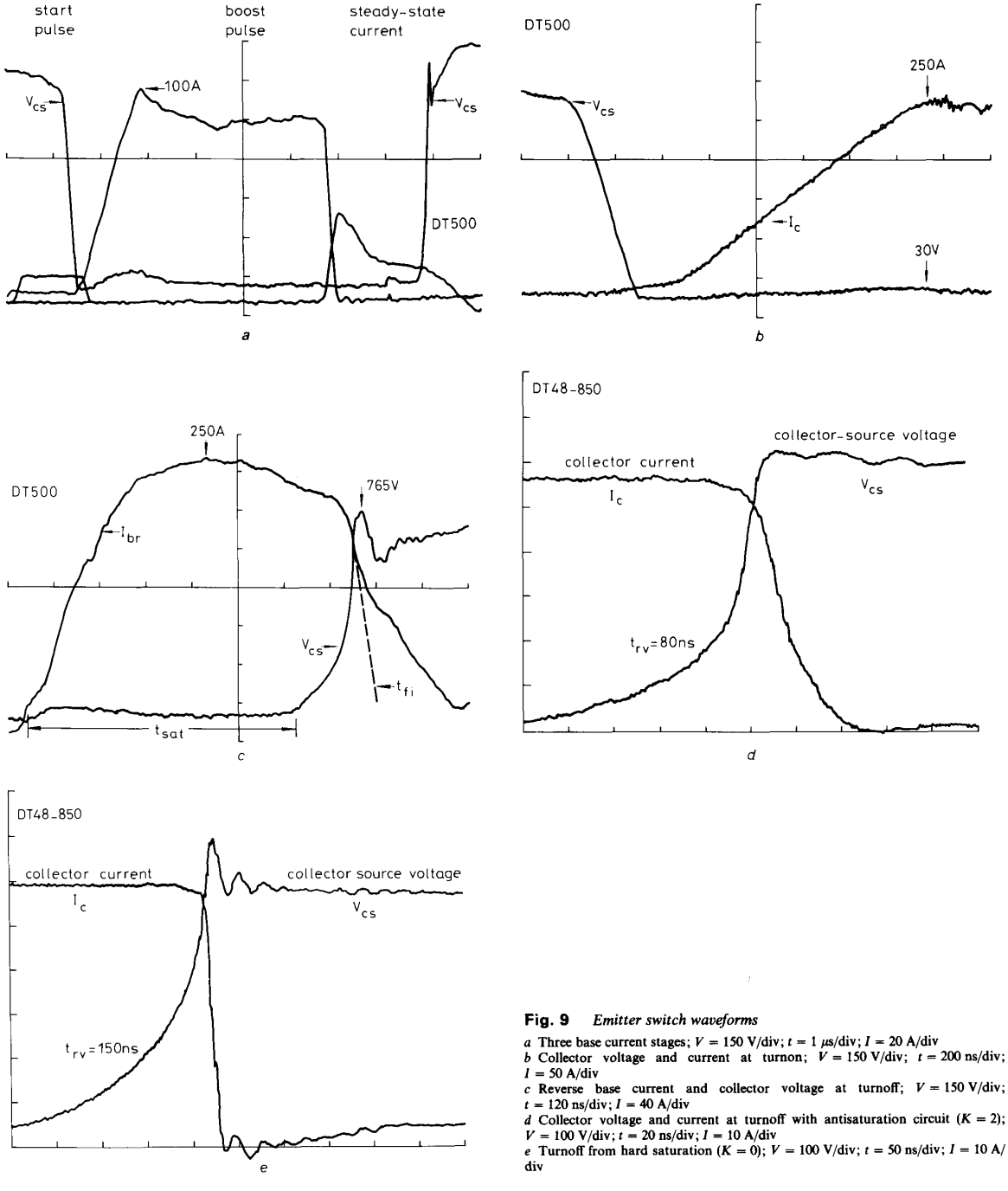

Fig. 9 *Emitter switch waveforms*

a Three base current stages; V = 150 V/div; t = 1 μs/div; I = 20 A/div
b Collector voltage and current at turnon; V = 150 V/div; t = 200 ns/div; I = 50 A/div
c Reverse base current and collector voltage at turnoff; V = 150 V/div; t = 120 ns/div; I = 40 A/div
d Collector voltage and current at turnoff with antisaturation circuit (K = 2); V = 100 V/div; t = 20 ns/div; I = 10 A/div
e Turnoff from hard saturation (K = 0); V = 100 V/div; t = 50 ns/div; I = 10 A/div

package is increased, with voltage ratings up to 9000 V available.

Fig. 12 shows the circuit diagram for a GTO thyristor cathode switch. No conventional *RCD* turnoff snubber is used across the GTO. Much of the circuitry is as for the emitter switched transistor, with the main simplifications being made to the turnon circuits and associated control logic.

No antisaturation shunt regulator is used. The current transformer is retained, not to provide gate current in the on state, but rather to provide reverse cathode current at turnoff. The anode circuit does not incorporate a saturable reactor as used with the emitter switch.

6.1 Turnon

Once T_c has been turned on and T_s turned off, switch turnon is started with a current pulse, via switch T_{01}, of 30 A for 6 μs, followed by a constant gate current of 2 A. The linear inductor $L_1 + L_2$, in the anode circuit, limits the initial di/dt to less than 500 A/μs. The secondary winding of the current transformer $CT_{1a,b}$ is shorted by MOSFET T_{b1}. Twenty per cent of the anode current

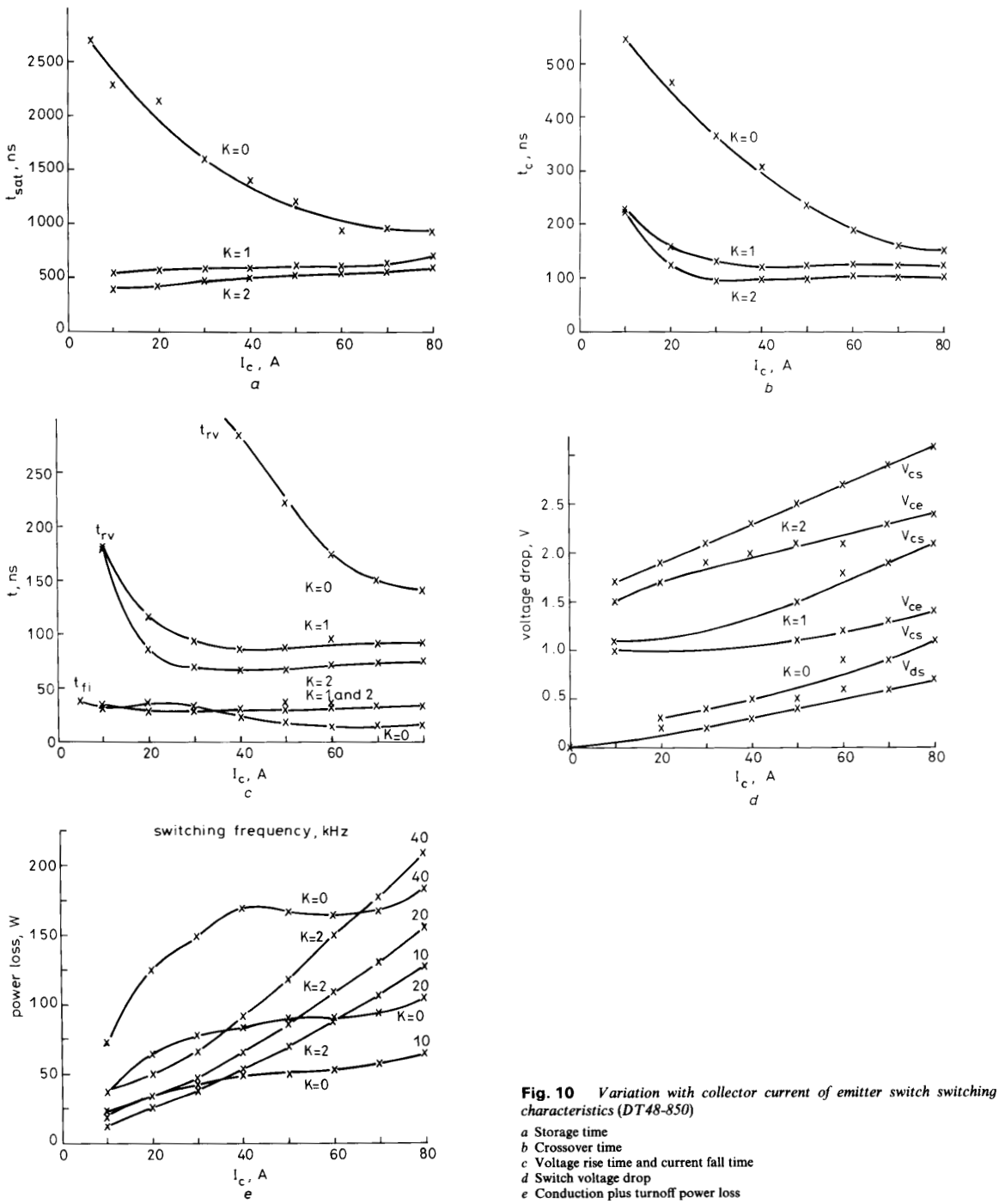

Fig. 10 *Variation with collector current of emitter switch switching characteristics (DT48-850)*

a Storage time
b Crossover time
c Voltage rise time and current fall time
d Switch voltage drop
e Conduction plus turnoff power loss

flows around the low-voltage loop, thus allowing a long on time before core saturation.

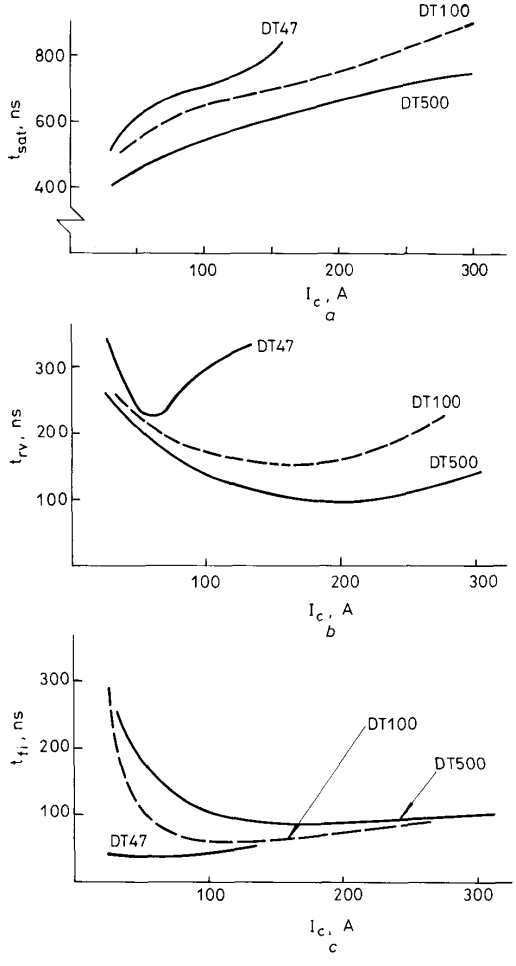

Fig. 11 *Collector current effects on switching characteristics for three power transistors at 700 V (K = 2)*

a Storage time
b Voltage rise time
c Current fall time

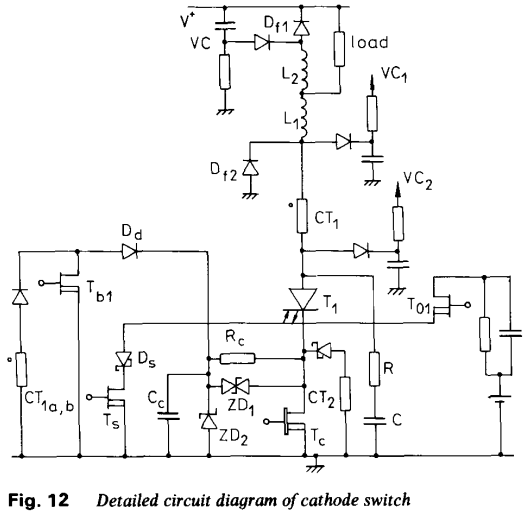

Fig. 12 *Detailed circuit diagram of cathode switch*

6.2 Turnoff

The cathode MOSFET T_c is turned off to open circuit the cathode and T_s is turned on to take up the anode current. The switch T_{b1} is turned off and a current $I_a/5$ is diverted via diode D_d to the cathode circuit. This current cuts off the cathode junction. Once the cathode has cut off, the GTO turns off like a *pnp* transistor in the V_{ceo} mode. The anode voltage and reverse gate current at turnoff are shown in Fig. 13.

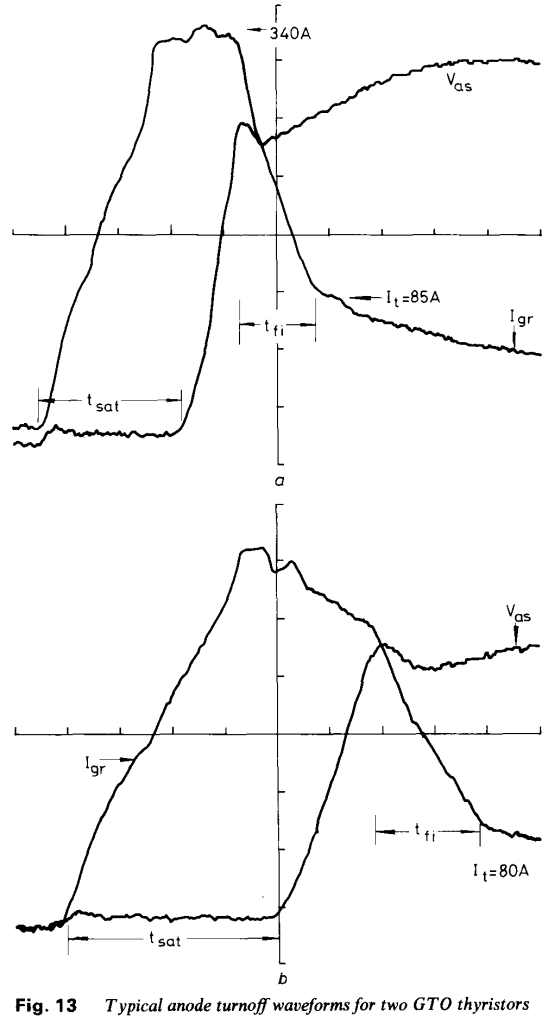

Fig. 13 *Typical anode turnoff waveforms for two GTO thyristors*

a DG306SE21 with anode shorts; V = 150 V/div; t = 200 ns/div; I = 50 A/div
b DGT304SE10; V = 150 V/div; t = 100 ns/div; I = 40 A/div

Additional reverse cathode current, 5 A for 4 μs, is provided by the current transformer CT_2. This current is used to cut off the cathode at low anode currents and after long on times. Under such conditions the current transformer CT_1 magnetising current may represent the full anode current. Hence no secondary current in $CT_{1a,b}$ is produced to aid cutoff of the cathode.

After saturation delay, the anode voltage rises beyond the rail voltage where it is controlled by the voltage clamp VC_2. Relatively low di/dts occur at turnoff, hence transient voltages due to stray inductance are lower than with the emitter switch.

The turnoff waveforms differ from those of the emitter switch, only in as far as an anode current tail occurs with the GTO thyristor.

7 Cathode switch performance

Two GTO thyristors were tested in the cathode switch configuration. Electrical characteristics are summarised in Table 2 of the Appendix.

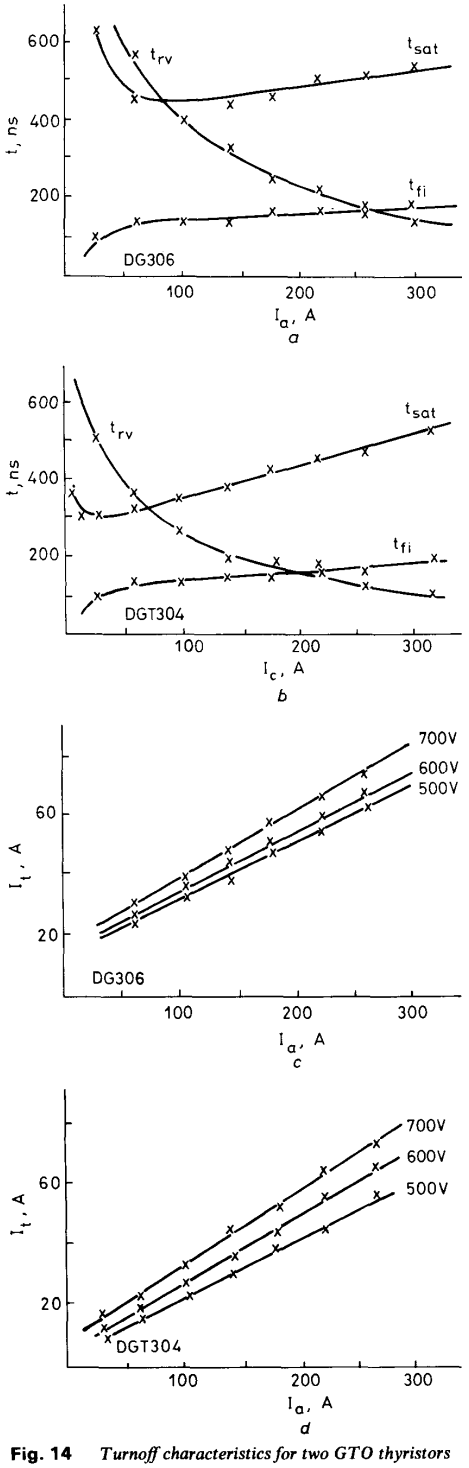

Fig. 14 *Turnoff characteristics for two GTO thyristors*

a, b Variation of storage time, voltage rise time and current fall time, with anode current magnitude

c, d Current tail magnitude variation with supply voltage and anode current prior to turnoff

The devices were tested at DC voltages between 500 V and 700 V and at currents from 30 A to 320 A, at a 16 kHz switching rate and a 50% on-state duty cycle. Fig. 13 shows the switching waveforms at 720 V DC and 300 A. The reverse gate current I_{gr} conducts the full anode current which comprises the current fall time and the current tail. The tail current occurs on the cathode switch for around 15 μs for the high voltage device, which has anode shorts. The tail current decays exponentially with a time constant τ of about 2.5 μs. A 6 μs tail current occurs with the low-voltage device, which does not have anode shorts.

It is seen in Fig. 13 that a snubberless anode voltage rate of rise in excess of 4000 V/μs is safely experienced. The device critical *dv/dt* rated limit with a conventional gate drive is 500 V/μs.

Fig. 14*a* and *b* show various turnoff switching times. The saturation delay t_{sat} at turnoff is significantly reduced, to less than 600 ns at 320 A. The voltage rise time t_{rv} decreases with increased anode current as the depletion layer capacitances are quickly charged. The cathode switch improves switchoff characteristics, but the initial magnitude of the tail current is increased. Figs. 14*c* and 14*d* show that the initial magnitude of the current tail I_t is proportional to both turnoff anode current and DC rail voltage [10, 12, 17].

8 Current tail

At turnoff the GTO tail current dominates power losses at higher frequencies and restricts the minimum off time. In very high voltage (>3000 V) GTO applications, tail loss may restrict the operating frequency to less than a few hundred Hertz. The gate and cathode at turnoff do not significantly affect the turnoff tail characteristics, since these terminals do not influence the wide, low concentration *n*-base region of the GTO. This high resistivity region is essential to produce a high voltage device and results in hole minority carrier lifetimes in excess of 100 μs. The *n*-base region affects both turnon and turnoff characteristics.

At turnon during a high *di/dt* the wide *n*-base makes the GTO look like an *npn* transistor. At specified initial *di/dt*, during freewheel diode reverse recovery, the GTO anode voltage rises, having fallen to near zero, in spite of a large initial gate current pulse. The inherent regenerative mechanisms of the thyristor respond too slowly because of the long carrier transit time associated with the *n*-base. For this reason a very high initial gate current pulse is used in an attempt to swamp *di/dt* effects.

The turnoff current tail, with initial value I_t is due to the *n*-base excess hole charge $\hat{Q}_0 = I_t \tau_F$ which remains after all the *p*-base charge is consumed. By the method of charge control parameters [16] the charge decays according to

$$\hat{Q}_h(t) = I_t \tau_F e^{-t/\tau_F} \tag{9}$$

where τ_F, the base forward transit time, is given by

$$\frac{1}{\tau_F} \triangleq \frac{1}{\tau_h} + \frac{1}{\tau_B} \tag{10}$$

τ_h is the hole lifetime and τ_B is given by eqn. 6. The magnitude of the anode diffusion current flow is therefore

$$I_a = |I_h(t)| = \left| \frac{d\hat{Q}_h(t)}{dt} \right| = I_t e^{-t/\tau_F} \tag{11}$$

The anode current is shown to be an exponential tail.

The hole charge $\hat{Q}_0$ should be minimised to reduce the tail current. This can be done in two ways. First by using the GTO near its voltage rating and secondly by using a GTO with an n-type anode junction buffer in the n-base.

9 Cascode switch control aspects

9.1 Fault protection for the emitter switch

Two fault detection and protection circuits are used. The first detects a freewheel diode or short circuit load fault, and the second circuit detects an overcurrent or base drive fault condition.

(i) At turnon the collector voltage fall is detected by the circuit in Fig. 7*a* and the current is controlled by L_1 and L_2 at 200 A/μs. For the freewheel diode D_{f1}, maximum recovery current occurs within 1.8 μs. The circuit in Fig. 7*b* is used to detect the instant of freewheel diode peak recovery current. If recovery is not detected within 1.8 μs (I_c = 360 A), and $v_{ce(sat)}$ is greater than 8 V, as detected by the circuit in Fig. 7*a*, either an overcurrent or diode failure is assumed. The base drive is latched off and a fault indicated.

(ii) During the switch on state, after the turnon transient, the collector voltage level is monitored by the circuit shown in Fig. 7*a*. After detection of the peak of the reverse recovery current by the circuit in Fig. 7*b*, the collector voltage is given a specified time (1 μs) to fall below 8 V. If the collector voltage does not fall to this level, or having done so subsequently exceeds 8 V, an overcurrent fault or base drive failure is assumed and the base drive is latched off and a fault indicated. Since the transistor is already in the quasisaturation region near the linear region, rapid turnoff occurs without saturation delay. The collector inductance, 3 μH, constrains the overcurrent within the FBSOA. Base drive failure is detected, when the collector voltage does not fall to less than 8 V within 0.5 μs, at turnon.

9.2 Load power factor considerations

Transistor turnon in three stages is applicable to loads that always absorb power. In a bridge configuration, with a reactive AC load, during a portion of an AC cycle, energy is returned to the supply. At such times, the freewheel diode in parallel with the switch to be turned on is conducting. The switch supports a slight negative voltage, a condition that can be detected by the circuit in Fig. 7*a*. Given that a diode fault condition has not been previously detected by the complementary switch, a modified 3 stage turnon sequence is initiated when the collector voltage rises above 8 V, as detected by the circuit in Fig. 7*a*. The base boost winding need not be activated as no diode recovery occurs. Diode recovery detection is not a prerequisite for turnon. Minimal current crossover distortion occurs and reverse transistor current through the collector junction, instead of the freewheel diode D_{f2}, is avoided.

In the case of the GTO, the normal turnon sequence is started once the circuit in Fig. 7*a* has detected the anode voltage reaching 8 V.

10 Test rig and measurement apparatus

The main components shown in Fig. 1 were held in a compact, water cooled, clamp arrangement, as shown in Fig. 15. Disc package GTOs and bipolar transistors were tested in a clamp, so devices were easily interchanged. The ground level cascode MOSFETs T_c (4 × T03P) were connected, without isolation, onto the cathode/emitter clamp aluminium bar, which was water-cooled. A copper busbar was used for the zero voltage rail. The shunt components, MOSFETs T_s (2 × T03P) and Chromium Schottky diodes D_s (2 × T03P) were connected without isolation to a second copper, 2 cm wide busbar. Minimal heatsinking is required for the shunt components because of their low on state duty cycle, being used only during the storage time and current fall time. The shunt circuit exploits the high pulse capabilities of the MOSFET and Schottky diode.

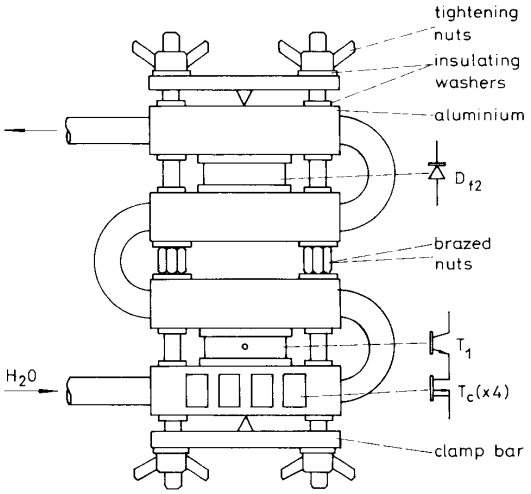

Fig. 15 *Construction arrangement of cascode switches*

The disc package freewheel diode was clamped so as to share the same two isolated studs as used in the clamp for the bipolar power switch. All four clamp bars are isolated from the two studs and clamp at each end. Minimal heatsinking was necessary because each of the four isolated island bars were water cooled. This efficient cooling method facilitated a compact arrangement which affords minimum stray inductance.

Current measurements were performed with a Tektronix AC current probe P6021, which has an upper cutoff frequency of 54 MHz and can measure 320 A before probe distortion. The probe was used in the base, or gate, lead where its 500 A μs rating was not exceeded. Voltage measurements were made with P6009, X100, 120 MHz probes and all voltage and current measurements were recorded by digital oscilloscope HP-54111D, which performs simultaneous sampling on two channels at 1 GHz.

RFI filters and isolation transformers with low interwinding capacitance were used on all-power supplies and the pulse generator. The gate/base drive and control circuitry was shielded with steel sheeting, with signals transmitted via feed through capacitors, twisted pairs and shielded cable as appropriate.

11 Alternative GTO thyristor cascode switches

11.1 Double-gate GTO thyristor

The 6000 V double gate GTO, with access to both the p-base and n-base was developed by Toshiba to reduce turnoff loss in high voltage GTOs [18]. An anode n-base n-buffer is used to attain a high voltage rating and to minimise the n-base lateral resistance. The device is suitable for use with a cascode switch in the anode as well as in the cathode as shown in Fig. 16.

Saturation delay with turnoff that uses only the *n*-base gate takes over 50 μs. As a consequence, accurate timing of turnoff via the *p*-base gate, in association with *n*-base gate turnoff is essential to minimise turnoff loss under a double gate turnoff mode. Using conventional gate turnoff drive circuits, turnoff loss is reduced by a factor of 20, with virtually no tail current, provided gate turnoff is suitably synchronised.

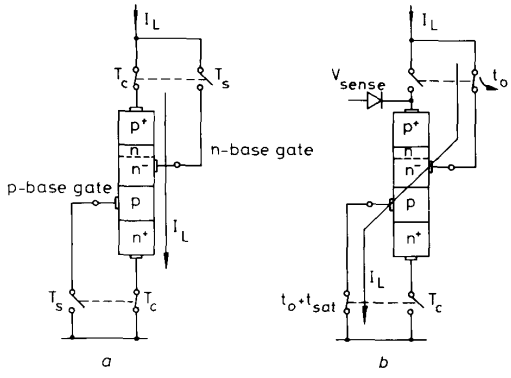

Fig. 16 *Current through the dual gate, dual cascode switch, GTO thyristor*

a Anode current in the on state
b Diversion of principal current through the two gates

The double gate GTO cascode switch as shown in Fig. 16 would behave like a *p–n* diode during recovery, just as with the emitter switched bipolar junction transistor at turnoff. The use of a cascode anode switch configuration would reduce the saturation delay by over an order of magnitude, from over 50 μs to less than 5 μs, because of a unity turnoff gain. Any *p*-base gate on drive current is removed during the saturation delay period. The subsequent rise in anode voltage, detected by the circuit in Fig. 7*a*, turns on the cathode switch. The remaining small *p*-base charge is removed rapidly as the cathode cuts off, without producing a current tail. Adaptive well synchronised turnoff of both gates may be achieved, minimising turnoff loss, independently of anode current magnitude and junction temperature.

11.2 Conventional p-base gate GTO thyristor

The anode shorted, defocussing structure of the conventional GTO is not optimal for either the single gate or the double gate cascode switch. Fig. 17*a* shows the conventional anode shorted structure during cathode switch turnoff. Since all the anode current is diverted to and extracted from the gate, the current filament is pulled undesirably to the *p–n–p* regions as shown. This action promotes anode injection. Interchange of the anode side *p* and *n* regions, as with the double gate GTO and as shown in Fig. 17*b* has two consequences:

(i) In the on state a true vertical *pnpn* thyristor section is in conduction, thereby minimising the on state voltage.

(ii) At turnoff, when the anode current is diverted to the two gates, the current filament is pulled towards a *p–n* region between the two gates as shown in Fig. 17*b*. Turnoff is similar to that of the emitter switched bipolar transistor, and occurs without any current focusing at either the cathode or anode junctions.

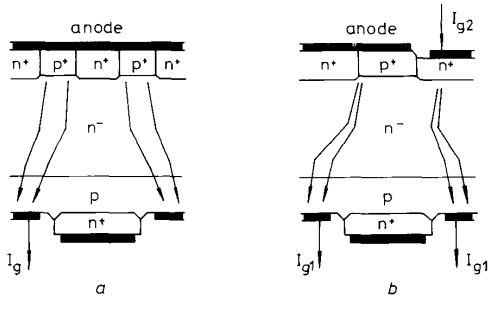

Fig. 17 *GTO thyristor anode current during turnoff*

a Conventional turnoff
b Modified GTO or double gate GTO thyristor turnoff

12 Conclusions

Design and performance aspects for the emitter switched bipolar transistor and the cathode switched GTO thyristor, have been presented. The cascode switch principle allows high power semiconductor switches to be used close to their maximum *V/I* rating at high frequencies and without the need for conventional *RCD* turnoff snubbers. Inductive turnon snubbing is essential at high frequencies because of freewheel diode recovery effects on the switching device.

The bipolar transistor emitter switch has been operated at over 230 kVA on a 720 V DC rail at a modulation frequency in excess of 50 kHz. The transistor is operated at its V_{cex} voltage rating. Switch minimum on and off times are circuit restricted rather than semiconductor device limited. Minimum off times of less than 3 μs are possible by using a dual voltage clamp to reset the magnetic components. Minimal transistor turnoff time is achieved by using a three stage optimal adaptive base current control technique that prevents excess base charge arising under all collector voltage and current conditions.

The snubberless cathode switch has been operated at 720 V DC, 320 A without any indication that these limits, particularly the voltage, cannot be significantly extended. At a 16 kHz operating frequency, the duty cycle is severely restricted by the GTO minimum on-time specification of 20 μs. The GTO thyristor minimum off time has been significantly reduced by the large reduction in the saturation delay time component. The tail current time component of the thyristor minimum off time is unaffected. At a switching frequency of 16 kHz the duty cycle variation is limited to 20%, from 32% to 52% on-time duties. At this frequency 85% of losses are contributed by the tail current. The reduced saturation delay time enhances GTO thyristor fault protection capabilities, decreasing the amount of anode circuit inductance required.

For each cascode switch type, a reduced current fall time, improved *dv/dt* rating and a reduced saturation delay are traded for increased circuit complexity and on state loss.

The cascode configuration can be utilised on static induction (field controlled) devices, where turnoff current gains are low at higher currents.

13 Acknowledgments

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14 References

1 CHEN, D.R., and JACKSON, B.: 'Effects of emitter-open switching on the turn-off characteristics of high-voltage power transistors', *IEEE Power Electron. Spec. Conf. Rec.*, 1980, **11**, pp. 147–154

2 SKANADORE, W.R.: 'A new high frequency power switching technology eliminates load-line shaping'. Proceedings of POWERCON 7, 1980, pp. 1–14

3 CLEMENTS, S., PELLY, B., RUTTONSHA, B., and TAYLOR, B.: 'High voltage, high frequency switching using a cascode connection of bipolar transistor and power mosfet', *IEEE*, 1982, **IAS-17**, pp. 1395–1405

4 SCHULTZ, W.: 'Drive optimisation for 1 kV off-line converter transistors'. Motorola Inc., Application note AN 951, 1985

5 CHEN, D., and WALDEN, J.P.: 'Application of emitter-open turn-off technique for high voltage inverter', *IEEE Power Electron. Spec. Conf. Rec.*, 1981, **12**, pp. 252–257

6 BOWLER, P., and JONES, D.: 'An evaluation of the limitations and capabilities of the cascode connected bimos switch'. IEE Power Electronics and Variable-speed Drives Conference, 1986, No. 264, pp. 15–19

7 ROBINSON, F.V.P., and WILLIAMS, B.W.: 'Emitter switching high-power transistors'. Proceedings of EPE 2, 1987, pp. 55–59

8 WIRTH, W.F.: 'The gate turn-off thyristor in the cascode configuration', *IEEE*, 1983, **IAS-18**, pp. 788–793

9 CLERC, C., RIOTTE, J.P., and ROJAT, G.: 'A new step towards the ideal switch: the GTO MOS cascode'. Proceedings of EPE 2, 1987, **1**, pp. 87–92

10 FLETCHER, R.G.: 'Switch behaviour of GTO cascode switches', *IEEE*, 1988, **IAS-23**, (1), pp. 633–637

11 GOODFELLOW, J.K., and WILLIAMS, B.W.: 'The bipolar transistor and GTO thyristor in a high power, high frequency cascode switch configuration', *IEEE Power Electron. Spec. Conf. Rec.*, 1988, **19**, pp. 695–702

12 GOODFELLOW, J.K., and WILLIAMS, B.W.: 'A high current ultrasonic thyristor cathode switch'. IEE Power Electronics and Variable-speed Drives Conference, 1988, No. 291, pp. 91–94

13 WILLIAMS, B.W., and GOODFELLOW, J.K.: 'A comparison of the GTO thyristor and bipolar transistor cascode switch'. IEE IES 14, 1988, **3**, pp. 661–666

14 ROBINSON, F.V.P., and WILLIAMS, B.W.: 'Active snubbing or passive snubbing for fast switches'. IEE IES 14, 1988, pp. 617–622

15 MACMURRAY, W.M.: 'Optimum snubbers for power semiconductors', *IEEE Trans.*, 1972, **IA**, (5), pp. 593–600

16 BAR-LEV, A.: 'Semiconductors and electronic devices' (Prentice-Hall International, 1979)

17 STEINKE, J.K.: 'Experimental results on the influence of the capacity of the snubber capacitor on the shape of the tail current of a GTO thyristor'. Proceedings of EPE 2, 1987, pp. 21–25

18 OGURA, T.: 'Double gate GTO thyristors'. Solid State Devices and Materials Conference, Aug. 1988, Japan, No. 20, pp. 37–40

15 Appendix

Table 1: Bipolar transistor characteristics

	V_{cex}, V	V_{cer}, V	I_{cont}, A	I_{cmax}, A	P_d, kW	Φ_d, mm	t_{sat}, μs	t_{fi}, μs
DT47-1050	1050	850	150	175	1.7	29.5	3.5	1.0
DT100-900	900	800	200	300	2.5	38	8.0	1.0
DT500-1000	1000	850	400	500	3.75	44	9.5	1.5

Table 2: GTO thyristor characteristics

	V_{drm}, V	V_d, V	I_{tav}, A	I_{tcm}, A	t_{sat} μs	t_{fi}, μs	dv/dt, V/μs	di/dt, A/μs	Φ_d, mm
DGT304SE10	1000	800	250	700	11	0.9	500	500	29.5
DG306SE21	2100	1800	210	600	12	2.0	500	300	29.5

Table 3: Electrical device data

D_{f1}	DSF5712 1200V 8 $\mu\Omega$ @ 300 A, −80 A/μs and 125°C
T_s	2 T03P IRF050 50 V 18 mΩ
T_c	4 TO3P IRF050 50 V 18 mΩ
T_{O1}	1 T0220 IRF642 200 V 0.22 mΩ
T_b	2 MTH30N20
T_2	2N6773
D_{as}	BA159
ZD_1	4 1.6KE15C
D_s	2 MBR3045PC 45 V 30 A
T_{b1}	1 MTH30N20
T_3	ZTX749
T_d	MTH40N10
ZD_2	4 1.6KE30